Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1038	716/12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:13
L2	571	716/13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:12
L3	529	716/14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:13
L4	738	716/16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:13
L5	819	716/17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:13
L6	4	(716/12).ccls. and (test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:17
L7	0	(716/13).ccls. and (test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:17
L8	0	(716/14).ccls. and (test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:17
L9	4	(716/16).ccls. and (test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:17
L10	5	(716/17).ccls. and (test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:17

L11	12	("716"/$).ccls. and (test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:17
L12	37	(test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:18
L13	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2) and ((target adj (routing adj resource))same (router adj (starting adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:20
L14	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2) and ((target adj (routing adj resource)) same (router adj (starting adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:21
L15	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2) and ((target adj (routing adj resource)) and (router adj (starting adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:22
L16	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and (routing adj resource$2) and ((target adj (routing adj resource)) and (router adj (start$4 adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:22
L17	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and ((target adj (routing adj resource)) and (router adj (start$4 adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:22
L18	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and ((routing adj resource) and (router adj (start$4 adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:23
L19	0	(test adj design) and ((programmable adj logic) or PLD of FPGA) and ((routing adj resource) same (router same (start$4 adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:24

L20	2	(test adj design) and ((programmable adj logic) or PLD of FPGA) and ((routing adj resource) and (router and (start$4 adj point)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:26
L21	0	((test adj design) and ((programmable adj logic) or PLD of FPGA) and ((routing adj resource) and (router and (start$4 adj point)))).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/06 11:26

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